

# Model 654C

## Advanced PLL HCMOS Clock

### Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 600fs Typical
- Advanced PLL Design w/ Low Fundamental Crystal
- Frequency Range 10 – 250MHz \*
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:  
5.0 × 3.2 × 1.2mm • 62.00mg

### Applications

- Broadcast Video Systems
- Storage Area Networking
- Broadband Access
- PCI Express
- Networking Equipment
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies  
 - 77.76MHz                      - 106.25MHz  
 - 100.00MHz                    - 125.00MHz  
 \* Check with factory for availability.

### Description

CTS Model 654C is a low cost, high performance PLL clock oscillator supporting HCMOS output. Employing the latest IC technology, M654C has excellent stability and low phase jitter performance.

### Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
654	C	XXX or XXXX	3	I	3	T
		Code      Frequency Product Frequency Code <sup>1</sup>		Code      Temp. Range C    -20°C to +70°C I    -40°C to +85°C		Code      Packing T      1k pcs./reel
	Code      Output C      HCMOS		Code      Stability 6      ±20ppm <sup>2</sup> 5      ±25ppm 3      ±50ppm		Code      Voltage 2      +2.5Vdc 3      +3.3Vdc	

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables.  
3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V
Supply Voltage	$V_{CC}$	$\pm 5\%$	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current	$I_{CC}$	Maximum Load	-	20	-	mA
Operating Temperature	$T_A$	-	-20 -40	+25	+70 +85	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-	-55	-	+125	$^{\circ}\text{C}$

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	$f_o$	-		10 - 250		MHz
Frequency Stability [Note 1]	$\Delta f/f_o$	-		20, 25 or 50		$\pm\text{ppm}$
Aging	$\Delta f/f_{25}$	First Year @ +25 $^{\circ}\text{C}$ , nominal $V_{CC}$	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Load	$C_L$	-	-	-	15	pF
Output Voltage Levels	$V_{OH}$ $V_{OL}$	CMOS Load	0.9 $V_{CC}$ -	- -	- 0.1 $V_{CC}$	V
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $C_L = 15\text{pF}$	-	5	10	ns
Start Up Time	$T_S$	Application of $V_{CC}$	-	3	5	ms
<b>Enable Function [Standby]</b>						
Enable Input Voltage	$V_{IH}$	Pin 1 Logic '1', Output Enabled	0.7 $V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 1 Logic '0', Output Disabled	-	-	0.3 $V_{CC}$	V
Disable Current	$I_{IL}$	Pin 1 Logic '0', Output Disabled	-	-	20	$\mu\text{A}$
Enable Time	$T_{PLZ}$	Pin 1 Logic '1', Output Enabled	-	-	5	ns
Phase Jitter, RMS	$t_{jrms}$	Bandwidth 12 kHz - 20 MHz	-	600	<1000	fs
Period Jitter, pk-pk	$p_{jpk-pk}$	-	-	3.0	-	ps
Period Jitter, RMS	$p_{jrms}$	-	-	30	-	ps

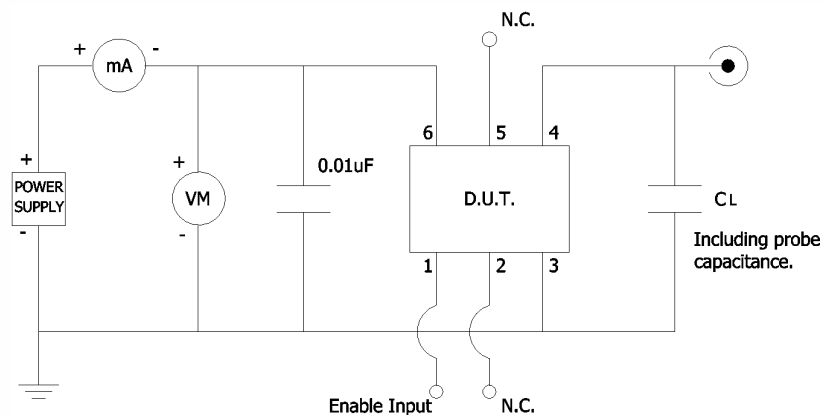
## Electrical Specifications

### Enable Truth Table

Pin 1	Pin 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

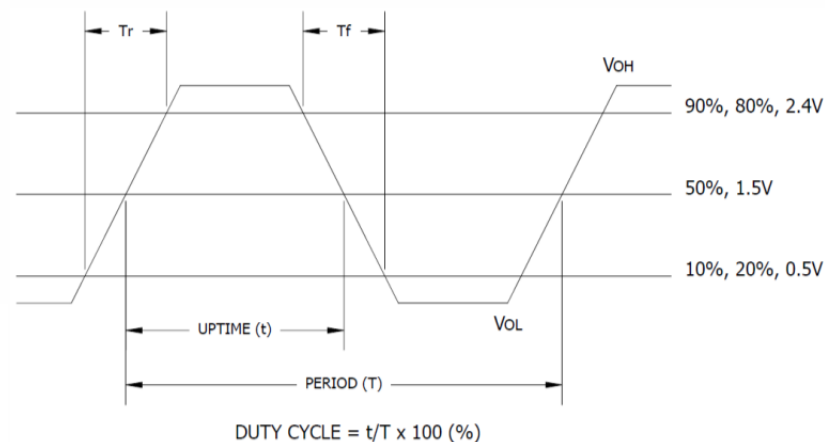
### Test Circuit

HCMOS



### Output Waveform

HCMOS

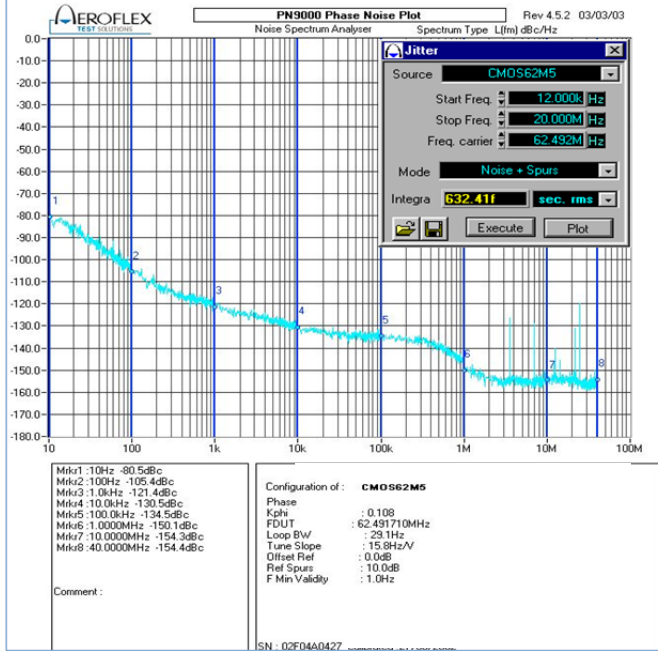


### Electrical Specifications

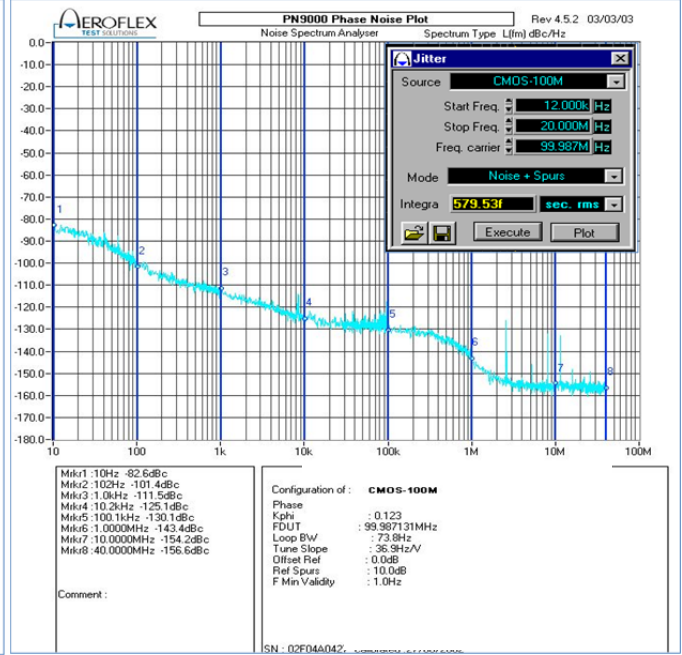
#### Performance Data

#### Phase Noise [typical]

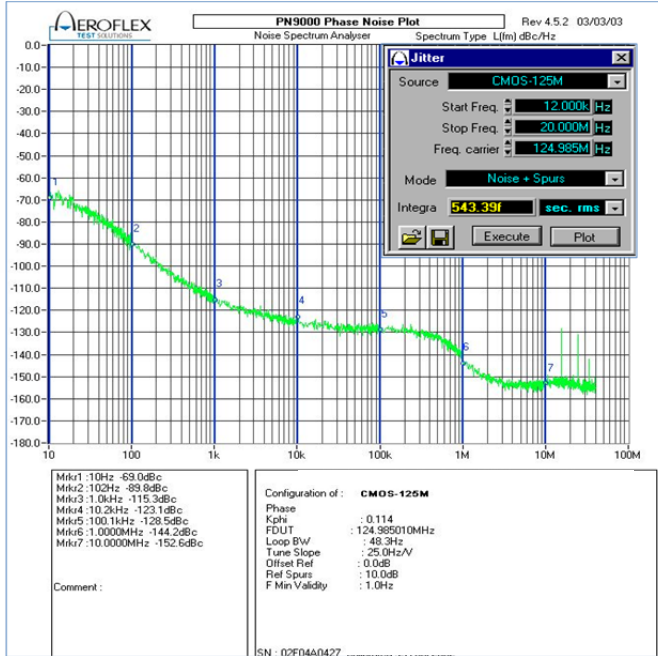
62.50MHz, HCMOS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



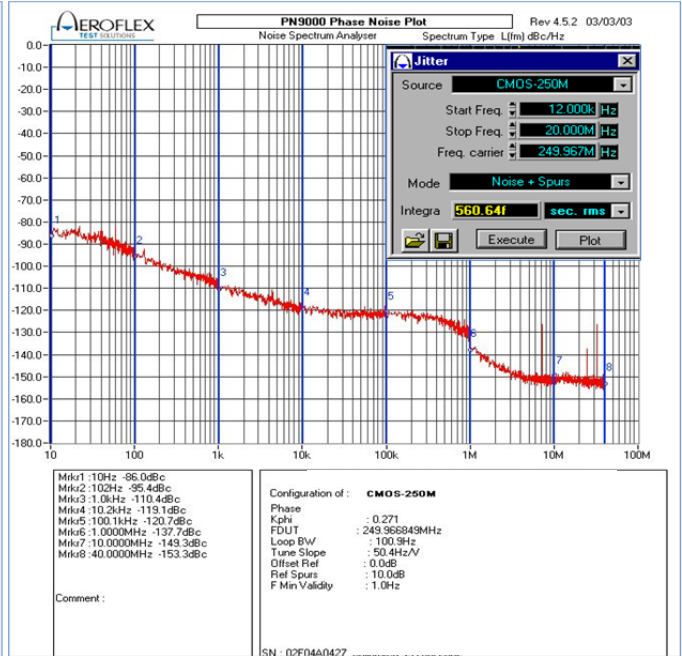
100.00MHz, HCMOS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



125.00MHz, HCMOS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



250.00MHz, HCMOS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



## Electrical Specifications

### Performance Data

#### Phase Noise Tabulated

Typical, HCMOS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>HCMOS @ 62.5MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-80.50	
		@ 100Hz	-105.40	
		@ 1kHz	-121.40	
	-	@ 10kHz	-130.50	dBc/Hz
		@ 100kHz	-134.50	
		@ 1MHz	-150.10	
		@ 10MHz	-154.30	
		@ 40MHz	-154.40	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	632.41	fs

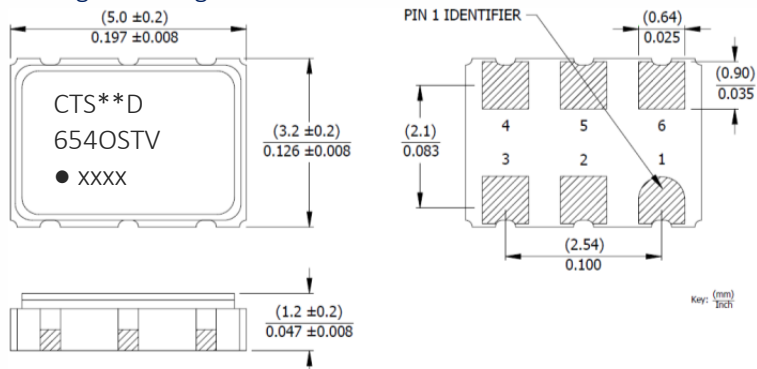
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>HCMOS @ 100.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-82.60	
		@ 100Hz	-101.40	
		@ 1kHz	-111.50	
	-	@ 10kHz	-125.10	dBc/Hz
		@ 100kHz	-130.10	
		@ 1MHz	-143.40	
		@ 10MHz	-154.20	
		@ 40MHz	-156.60	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	579.53	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>HCMOS @ 125.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-69.00	
		@ 100Hz	-89.80	
		@ 1kHz	-115.30	
	-	@ 10kHz	-123.10	dBc/Hz
		@ 100kHz	-128.50	
		@ 1MHz	-144.20	
		@ 10MHz	-152.60	
		@ 40MHz	-153.00	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	543.39	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>HCMOS @ 250.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-86.00	
		@ 100Hz	-95.40	
		@ 1kHz	-110.40	
	-	@ 10kHz	-119.10	dBc/Hz
		@ 100kHz	-120.70	
		@ 1MHz	-137.70	
		@ 10MHz	-149.30	
		@ 40MHz	-153.30	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	560.64	fs

## Mechanical Specifications

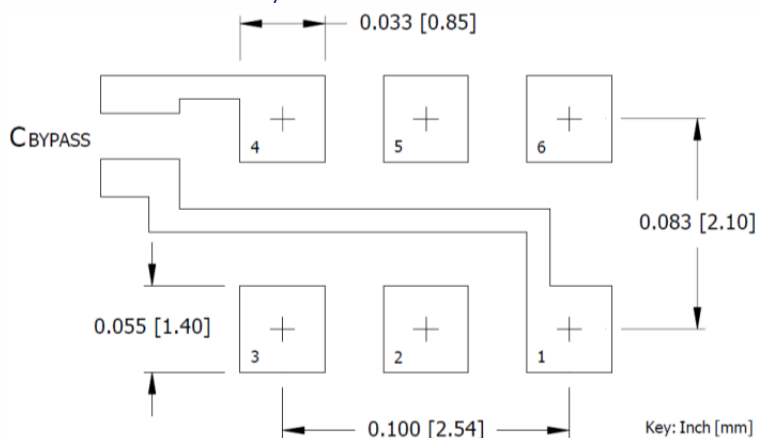
### Package Drawing



### Marking Information

- \*\* - Manufacturing Site Code.
  - D - Date Code. See Table I for codes.
  - O - Output Type; C = HCMOS.
  - ST - Frequency Stability/Temperature Code. [Refer to Ordering Information]
  - V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
  - xxxx - Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater
- [See document 016-1454-0, Frequency Code Tables.]

### Recommended Pad Layout



### Notes

- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

### Pin Assignments

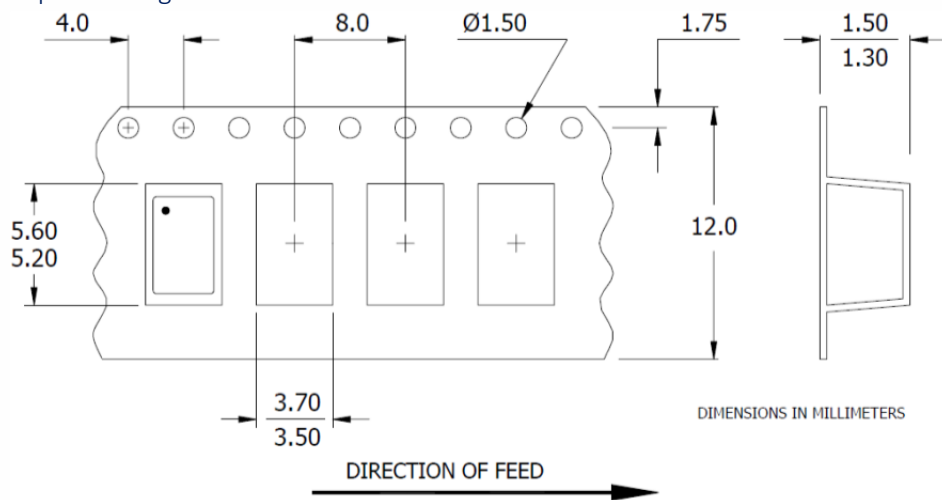
Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V <sub>CC</sub>	Supply Voltage

Table I - Date Code

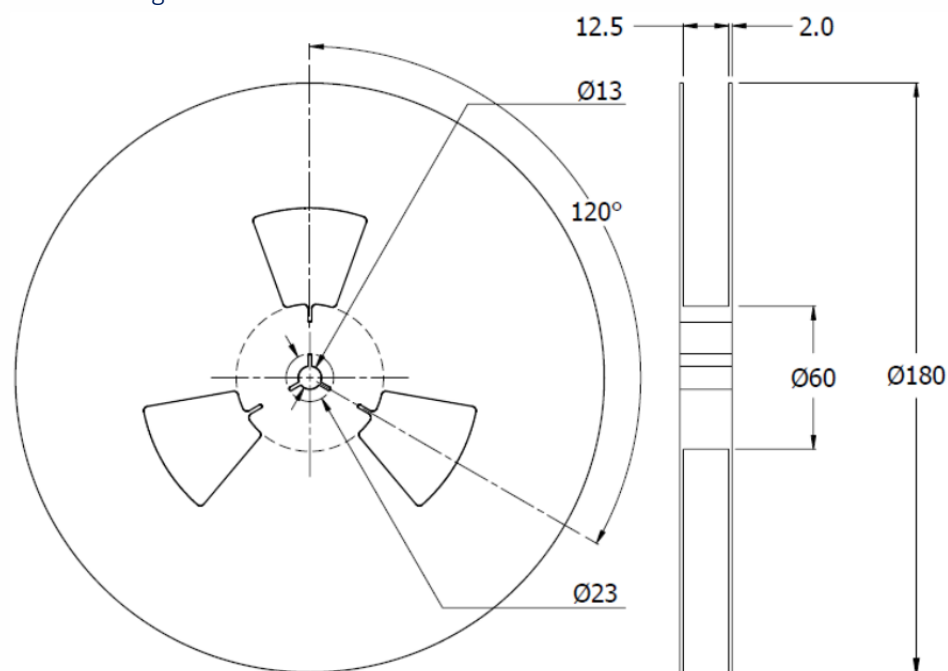
YEAR		MONTH														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC			
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

### Packaging - Tape and Reel

Tape Drawing



Reel Drawing



#### Notes

1. Device quantity is 1k pieces per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.